

line 11, after "VSUM" delete "may";
 line 12, before "set" delete "be" and insert --is--;
 after "set" delete "equal to zero";
 line 16, after "to" insert --the--;
 line 18, before "than" delete "greater" and insert --
 less--; and
 line 23, before "than" delete "less" and insert --
 greater--.

Page 16, line 10, after "and" delete "J²" and insert --J₂--.

IN THE CLAIMS:

Please delete claims 2-3 and 15-16 without prejudice.

Please amend the claims as follows:

1. (amended) A direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source supplying a current to the summing node and being connected to a power supply voltage[, wherein the current at the summing node is equal to zero when the power supply voltage is equal to a preselected voltage],
wherein the currents sources supply currents according to a bandgap equation:

$$K_1(V_{CC} - V_T) + K_1 V_T = K_2 V_{BE} + K_3 (kT/q)$$

where V_{CC} is the power supply voltage, V_T is the threshold voltage, V_{BE} is a base emitter voltage, and kT/q is equal to a thermal voltage where k is Boltzman's constant, T is the temperature in kelvin, q is the electronic charge, and K₁, K₂, and K₃ are constants; and

an indicator circuit having an input connected to the

18 summing node and generating a logical signal at an output,
19 responsive to voltage changes in the summing node.

1 4. (amended) [The direct current sum bandgap voltage
2 comparator of claim 3,] A direct current sum bandgap voltage
3 comparator comprising:

4 a summing node;

5 a plurality of current sources connected to the summing
6 node, each current source supplying a current to the summing
7 node and being connected to a power supply voltage; and

8 an indicator circuit having an input connected to the
9 summing node and generating a logical signal at an output,
10 responsive to voltage changes in the summing node, wherein the
11 currents sources supply currents according to a bandgap
12 equation:

$$K_1 (V_{CC} - V_T) + K_1 V_T = K_2 V_{BE} + K_3 (kT/q)$$

13
14 where V_{CC} is the power supply voltage, V_T is the threshold
15 voltage, V_{BE} is a base emitter voltage, and kT/q is equal to a
16 thermal voltage where k is Boltzman's constant, T is the
17 temperature in kelvin, q is the electronic charge, and K_1 , K_2 ,
18 and K_3 are constants and wherein the plurality of current
1 [mirrors] sources comprises four current mirrors.

2 4. (amended) The direct current sum bandgap voltage
3 comparator of claim 3, wherein the first current mirror
4 includes a plurality of transistors and supplies a current to
5 the summing node defined by $K_1(V_{CC} - V_T)$ [, where V_{CC} is the power
6 supply voltage and V_T is a threshold voltage in the first
current mirror].

1 5. (amended) The direct current sum bandgap voltage
2 comparator of claim 4, wherein the second current mirror
3 includes a plurality of transistors and supplies a current to

the summing node defined by $K_1 V_T$ [, where V_T is a threshold voltage in the second current mirror].

8. (amended) The direct current sum bandgap voltage comparator of claim 5, wherein the third current mirror includes a plurality of transistors and supplies a current to the summing node defined by $K_2 V_{BE}$ [, where V_{BE} is a base-emitter voltage defined by a selected transistor in the third current mirror].

9. (amended) The direct current sum bandgap voltage comparator of claim 8 further comprising a clamping circuit connected to the summing node, wherein a voltage swing for the summing node, responsive to changes in current supplied by the current mirrors, may be set between selected voltages [for the summing node].

10. (amended) The direct current sum bandgap voltage comparator of claim 8 further comprising a cascode stage [interposed] located between the summing node and the current mirrors.

14. (amended) A zero power circuit comprising:

a first circuit;

a direct current sum bandgap voltage comparator comprising:

a summing node;

a plurality of current sources connected to the summing node, each current source supplying a current to the summing node and being connected to a power supply voltage [, wherein the current at the summing node is equal to zero when the power supply voltage is equal to a preselected voltage], wherein the current sources supply according to a bandgap equation:

12
$$K_1 (V_{CC} - V_T) + K_1 V_T = K_2 V_{BE} + K_3 (kT/q)$$

13 where V_{CC} is the power supply voltage, V_T is the threshold
14 voltage, V_{BE} is a base emitter voltage, and kT/q is equal to
15 the thermal voltage, where k is Boltzman's constant, T is the
16 temperature in kelvin, q is the electronic charge, and K_1 , K_2 ,
17 and K_3 , are constants.
18 ; and

19 an indicator circuit having an input connected to
20 the summing node and generating a logical signal at an output,
21 responsive to changes in the summing node; and
22

23 a switching circuit for providing power to the first
24 circuit from a primary power supply and a secondary power
25 supply, the switching circuit being connected to the output of
26 the indicator circuit, wherein power from the primary power
27 supply is supplied to the first circuit if the logical signal
28 indicates that the power supply voltage is equal to or greater
29 than the preselected voltage and power from the secondary
30 power supply is supplied to the first circuit if the power
31 supply voltage is less than the preselected voltage.

1 17. (amended) [The zero power circuit of claim 16,] A zero
2 power circuit comprising:

3 a first circuit;

4 a direct current sum bandgap voltage comparator
5 comprising:

6 a summing node;

7 a plurality of current sources connected to the
8 summing node, each current source supplying a current to the
9 summing node and being connected to a power supply voltage-;

10 and

11 an indicator circuit having an input connected to
12 the summing node and generating a logical signal at an output,
13 responsive to changes in the summing node; and

14 a switching circuit for providing power to the first
15 circuit from a primary power supply and a secondary power
16 supply, the switching circuit being connected to the output of
17 the indicator circuit, wherein power from the primary power
18 supply is supplied to the first circuit if the logical signal
19 indicates that the power supply voltage is equal to or greater
20 than the preselected voltage and power from the secondary
21 power supply is supplied to the first circuit if the power
22 supply voltage is less than the preselected voltage, wherein
23 the current sources supply according to a bandgap equation:

24
$$f \quad K_1 (V_{CC} - V_T) + K_1 V_T = K_2 V_{BE} + K_3 (kT/q)$$

25 where V_{CC} is the power supply voltage, V_T is the threshold
26 voltage, V_{BE} is a base emitter voltage, and kT/q is equal to
27 the thermal voltage, where k is Boltzman's constant, T is the
28 temperature in kelvin, q is the electronic charge, and K_1 , K_2 ,
29 and K_3 , are constants and wherein the plurality of current
30 sources comprises four current mirrors.

1 119 18. (amended) The zero power circuit of claim [16] 119
2 wherein the secondary power supply is a battery.

1 116 19. (amended) The zero power circuit of claim 14, wherein the
2 first current mirror includes a plurality of transistors and
3 supplies a current to the summing node defined by $K_1 (V_{CC} - V_T)$ [,
4 where V_{CC} is the power supply voltage and V_T is a threshold
5 voltage in the first current mirror].

1 117 20. (amended) The zero power circuit of claim 14, wherein the
2 second current mirror includes a plurality of transistors and
3 supplies a current to the summing node defined by $K_1 V_T$ [, where
4 V_T is a threshold voltage in the second current mirror].

1718
1 ~~21~~. (amended) The zero power circuit of claim ~~20~~¹⁷, wherein the
2 third current mirror includes a plurality of transistors and
3 supplies a current to the summing node defined by $K_2 V_{BE}$ [, where
4 V_{BE} is a base-emitter voltage defined by a selected transistor
5 in the third current mirror].

Cont'd
A5
1 ~~23~~²⁰. (amended) The zero power circuit of claim ~~22~~¹⁹ further
2 comprising a clamping circuit connected to the summing node,
3 wherein a voltage swing for the summing node, responsive to
4 changes in current supplied by the current mirrors, may be set
5 between selected voltages [for the summing node].

19
1 ~~24~~²². (amended) The zero power circuit of claim ~~22~~¹⁹ further
2 comprising a cascode stage [interposed] located between the
3 summing node and the current mirrors.

Please add the following new claims:

Sub
C6
1 --27. A direct current sum bandgap voltage comparator
2 comprising:

3 a summing node;

4 a plurality of current sources connected to the summing
5 node and directly connected to a power supply voltage, each
6 current source supplying a current to the summing node,
7 wherein the summing node voltage level is responsive to the
8 currents supplied; and

9 an indicator circuit having an input connected to the
10 summing node, wherein the indicator circuit is responsive to
11 changes in the summing node voltage level and generates at an
12 output a logical signal at one state when the summing node
13 voltage level is greater than a predetermined value and
14 generates the logical signal at the output at another state
15 when the summing node voltage level is less than the
16 predetermined value, the predetermined value corresponding to